Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L3	156	regulat$3 same (drain source) same ("flash memory" eerpom)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/16 12:01
L4	2616	stress same regulator	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/16 12:01
L5	79	stress same regulator same test	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/16 12:02
L6	3	stress same regulator same test same drain	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/16 12:05
L7	119	regulator same test same drain	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/16 12:06
L8	4	regulator same test same drain and (eeprom "flash memory")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/16 12:30
L9	12	"regulated drain voltage" and (eeprom "flash memory")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/16 12:32
L10	2	9 and test$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/16 12:32
L11	3592	(365/200).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/16 13:35
L12	1794	(365/189.09).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/16 13:38

S3	3004	(365/201).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/21 09:54
S4	593	(365/185.09).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/21 10:07
S5	87	S3 and S4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/12/21 10:07
S6	2	S5 and regulator	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/12/21 10:07
S8	3210	(flash eeprom) and "test mode"	US-PGPUB; USPAT; USOCR	OR	ON	2004/12/21 10:15
S9	80	(flash eeprom) and "test mode circuit"	US-PGPUB; USPAT; USOCR	OR	ON	2004/12/21 14:05
S10	3	(flash eeprom) and "test mode circuit" and regulator	US-PGPUB; USPAT; USOCR	OR	ON	2004/12/21 10:16
S11	105	((flash eeprom) and test$3).ti.	US-PGPUB; USPAT; USOCR	OR	ON	2004/12/21 14:09
S12	46	((flash eeprom) and test$3).ti. and memory	US-PGPUB; USPAT; USOCR	OR	ON	2004/12/21 14:23
S13	5	yumoto.in. and test$3.ti.	US-PGPUB; USPAT; USOCR	OR	ON	2004/12/21 14:52
S16	8	("4855956").URPN.	USPAT	OR	ON	2004/12/27 11:24
S17	0	(eeprom "flash memory" "floating gate") and test$3 same mode same "all"	USPAT	OR	ON	2004/12/27 11:25
S18	4228	(eeprom "flash memory" "floating gate") and test$3 same mode	USPAT	OR	ON	2004/12/27 11:25
S19	0	(eeprom "flash memory" "floating gate") and test$3 same mode same all	USPAT	OR	ON	2004/12/27 11:25
S20	0	(eeprom "flash memory" "floating gate") and test$3 and all with ("word line" wordline)	USPAT	OR	ON	2004/12/27 11:31

S21	3194	external same monitor$4 same test$3	USPAT	OR	ON	2004/12/27 12:13
S22	380	S21 and (eeprom "flash memory" "floating gate")	USPAT	OR	ON	2004/12/27 11:32
S23	137	S22 and pad	USPAT	OR	ON	2004/12/27 11:32
S24	41	(S21 same pad) and (eeprom "flash memory" "floating gate")	USPAT	OR	ON	2004/12/27 11:33
S25	49012	(eeprom "flash memory" "floating gate")	USPAT	OR	ON	2004/12/27 11:50
S26	666	S25 same regulator	USPAT	OR	ON	2004/12/27 11:35
S27	151	S25 same regulator same (drain source)	USPAT	OR	ON	2004/12/27 11:48
S29	90	S25 same stress same test$3	USPAT	OR	ON	2004/12/27 11:50
S30	24	S25 same stress same test$3 same high near3 (voltage field)	USPAT	OR	ON	2004/12/27 11:50
S31	13	S25 same stress same test$3 same high near3 (voltage field) same gate	USPAT	OR	ON	2004/12/27 12:09
S32	4	high near3 gate near3 voltage with stress with test$3	USPAT	OR	ON	2004/12/27 12:11
S33	154	external same monitor$4 same test$3 same pad	USPAT	OR	ON	2004/12/27 12:15
S34	33	external with monitor$4 with test$3 with pad	USPAT	OR	ON	2004/12/27 12:45
S37	244	pad near5 (monitor$3 test$3) and test$3 with address with (pin terminal)	US-PGPUB; USPAT; USOCR	OR	ON	2005/01/03 11:59
S38	53	S37 and (eeprom eprom "flash memory" floating-gate "floating gate")	US-PGPUB; USPAT; USOCR	OR	ON	2005/01/03 11:57
S39	146	pad near5 (monitor$3 test$3) and test$3 with address near3 (pin terminal)	US-PGPUB; USPAT; USOCR	OR	ON	2005/01/03 12:00
S40	31	pad near5 (monitor$3 test$3) and test$3 with address near3 (pin terminal) and (eeprom eprom "flash memory" floating-gate "floating gate")	US-PGPUB; USPAT; USOCR	OR	ON	2005/01/03 12:33
S42	4502	accelerat$3 same test$3 same (life fatigue endurance)	US-PGPUB; USPAT; USOCR	OR	ON	2005/01/03 12:39
S43	6	accelerat$3 same test$3 same (life fatigue endurance) same (eeprom "flash memory" floating-gate "floating gate")	US-PGPUB; USPAT; USOCR	OR	ON	2005/01/03 12:40
S44	11	externally near5 monitor$3 with test$3 near3 voltage	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/15 08:33

S45	2	monitor$3 with externally with "mode signal" with test$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/15 08:36
S46	3051	(365/201).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/15 08:51
S47	5	"address buffer" and (eeprom "flash memory") and "test mode" and pad and oxide same stress same test$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/15 09:28
S48	14	"address buffer" and (eeprom "flash memory") and "test mode circuit" and pad	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/15 09:46
S50	67	oxide same stress same test and (eeprom "flash memory")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/15 09:48
S52	9	stress adj (test voltage) same (eeprom eprom flash) and "address buffer" and "test mode"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/15 10:24
S53	242	(365/189.03).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/16 06:55
S54	27	S53 and address same "test mode"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/16 06:56
S56	12	("4601034" | "4654849" | "4719599" | "4812675" | "4855621" | "4860259" | "4942319" | "4951254" | "4956818" | "4965768" | "4987325" | "4996672"). PN.	US-PGPUB; USPAT; USOCR	OR	ON	2005/03/16 07:14
S58	12	("5327363" | "5535164" | "5548553" | "5568437" | "5588006" | "5617531" | "5640354" | "5640404" | "5640509" | "5661729" | "5661732" | "5689466"). PN.	US-PGPUB; USPAT; USOCR	OR	ON	2005/03/16 07:16

S59	4	S58 and monitor$3	US-PGPUB; USPAT; USOCR	OR	ON	2005/03/16 07:19
S61	91	"stress test" same mode same address	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/16 07:26
S62	20	"stress test" same mode same address and (eeprom "flash memory")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/16 08:44
S63	13	externally near3 (monitor$3 verif$4) with test near3 mode near3 (signal voltage entry enter$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/16 08:53
S64	19	"stress test" and "test mode" near3 (entry enter$3) with address near3 (bit terminal pad signal voltage)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/16 09:05
S65	8	"bist detector" same address	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/16 09:15
S66	16	"stress test" same bist	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/16 09:29
S67	624	"test mode circuit"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/16 09:29
S68	27	S67 same "stress"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/16 09:35
S69	9	test$3 near5 monitor$3 near5 (terminal pad pin) same stress	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/16 10:04

S70	1221	test$3 near5 monitor$3 near5 (terminal pad pin)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/16 10:04
S71	238	S70 same pad	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/16 10:04
S72	25	S70 same pad same address	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/16 10:07
S73	59	S70 same address	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/16 10:11
S74	59	stress same test$3 same mode same (enter$3 entry activat$3 enabl$3) same address adj3 (line signal pin terminal pad)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/16 10:16
S75	14	S74 and monitor$3 near3 (pin pad terminal)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/16 11:48